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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Cheng et al.

Application No. 10/749,283

Filed: December 30, 2003

Confirmation No. 9850

For: BUILT-IN SELF-ANALYZER FOR
EMBEDDED MEMORY

Examiner:

Art Unit: 2133

Attorney Reference No. 1011-66273-01

CERTIFICATE OF MAILING

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Attorney
for Applicants

Date Mailed

3/16/05

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PURSUANT TO 37 C.F.R. § 1.97(b)(3)**

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Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

If the present application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55). Applicants will provide copies of such patents upon request.

Applicants filed this Information Disclosure Statement ("IDS") before the mailing date of a first Office action on the merits. As a result, no fee should be required to file this IDS.

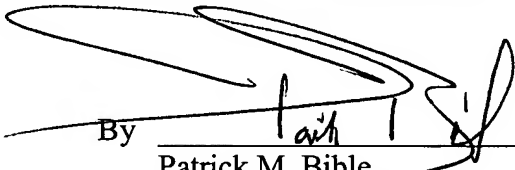
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The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

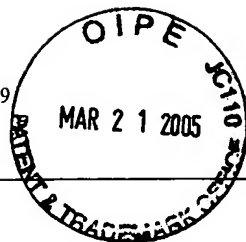
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Attorney Docket Number	1011-66273-01
Application Number	10/749,283
Filing Date	December 30, 2003
First Named Inventor	Cheng
Art Unit	2133
Examiner Name	

Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
		Bhavsar, "An Algorithm for Row-Column Self-Repair of RAMs and Its Implementation in the Alpha 21264", Proc. IEEE Int'l Test Conference, pp. 311-318 (1999).
		Haddad et al., "Increased Throughput for the Testing and Repair of RAM's with Redundancy," <i>IEEE Transactions on Computers</i> , Vol. 40, No. 2, pp. 154-166 (February 1991).
		Horstmann et al., "Metastability Behavior of CMOS ASIC Flip-Flops in Theory and Test," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 24, No. 1, pp. 146-157 (February 1989).
		Kawagoe et al., "A Built-in Self-repair Analyzer (CRESTA) for Embedded DRAMs", Proc. IEEE Int'l Test Conference, pp. 567-574 (2000).
		Kim et al., "Built In Self Repair for Embedded High Density SRAM", <i>Proc. IEEE Int'l Test Conference</i> , pp. 1112-1119 (1998).
		Nakahara et al., "Built in Self-test for GHz Embedded SRAMs Using Flexible Pattern Generator and New Repair Algorithm", <i>Proc. IEEE Int'l Test Conference</i> , pp 301-310 (1999).
		Powell et al., "BIST for Deep Submicron ASIC Memories with High Performance Application", <i>ITC 2003</i> (to appear)
		Shoukourian et al., "An Approach for Evaluation of Redundancy Analysis Algorithms", <i>Proc. IEEE MTDT Workshop</i> , San Jose, pp. 51-55, 2001
		Venkatesh et al., "A Fault Modeling Technique to Test Memory BIST Algorithms", <i>Memory Technology, Design and Testing, Proc. of the 2002 IEEE Int'l Workshop</i> , pp. 109-116 (2002).
		Zorian, "Embedded Memory Test & Repair: Infrastructure IP for SOC Yield", <i>Proc. IEEE Int'l Test Conference</i> , pp. 340-349 (2002).

**EXAMINER
SIGNATURE:**

**DATE
CONSIDERED:**

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.